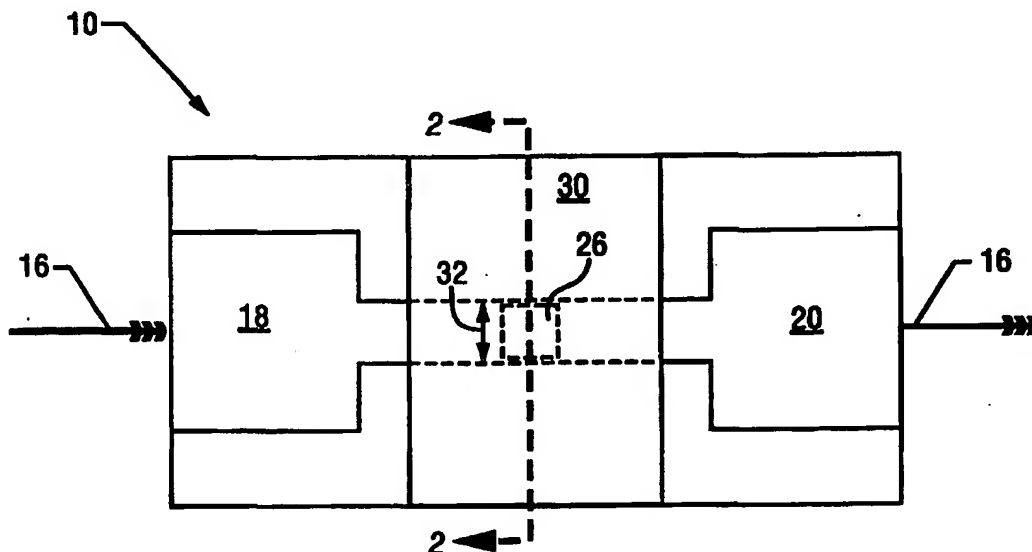




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(54) Title: SINGLE-ELECTRON FLOATING-GATE MOS MEMORY



**(57) Abstract**

A Single Electron MOS Memory (SEMM), in which one bit of information is represented by storing only one electron, has been demonstrated at room temperature. The SEMM is a floating gate Metal-Oxide-Semiconductor (MOS) transistor in silicon with a channel width (about 10 nanometers) which is smaller than the Debye screening length of a single electron stored on the floating gate (26), and a nonoscale polysilicon dot (about 7 nanometers by nanometers by 2 nanometers) as the floating gate which is positioned between the channel and the control gate (30). An electron stored on the floating gate (26) can screen the entire channel from the potential on the control gate, and lead to: (i) a discrete shift in the threshold voltage; (ii) a staircase relation between the charge voltage and the shift; and (iii) a self-limiting charge process. The structure and fabrication of the SEMM is well adapted to the manufacture of ultra large-scale integrated circuits.

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**SINGLE-ELECTRON FLOATING-GATE MOS MEMORY****I. PATENT RIGHTS STATEMENT**

This invention was partially funded by the Department of the Navy (Grant Nos.  
5 N/N00014-96-1-0160; N/N00014-93-1-0082; N/N00014-96-1-0788), the Department of the  
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ECS-9522201). The Government may have certain rights in this invention.

**II. TECHNICAL FIELD**

10 This invention relates generally to a data storage device, and more specifically to a  
data storage device capable of representing a bit of information (i.e., a logic '0' or a logic '1')  
by storing and detecting a single charge carrier during room-temperature operation.

**III. BACKGROUND OF THE INVENTION**

15 To increase the storage density of semiconductor memories, the size of memory cells  
must be reduced. Smaller memory cells also lead to faster speeds and lower power  
consumption.

A widely-used semiconductor memory is the "floating gate" memory. A floating gate  
memory has a floating gate interposed between a channel and a control gate. Information is  
20 represented by storing a plurality of charges (e.g., hundreds of thousands) on the floating  
gate. The information stored in a floating gate memory can be determined because differing  
amounts of charge on the floating gate will shift the threshold voltage of the transistor. A  
relatively low threshold voltage (e.g., no excess charges on the floating gate) can be used to

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represent a stored logic '0', and a relatively high threshold voltage (e.g., a plurality of charges on the floating gate) can be used to represent a stored logic '1.' For a detailed discussion of floating gate memories, the reader is referred to S.M. Sze, "Physics of Semiconductor Devices," John Wiley & Sons, pp. 496-497 (1981), which is incorporated into this application  
5 by reference in its entirety.

Recently, MOS memory cells have been fabricated which are capable of storing and detecting the presence or absence of a single charge to represent either a logic '1' or logic '0.' A device capable of this feat is referred to as a Single Electron MOS Memory (SEMM).

A previous SEMM design, disclosed in Kazuo Yano et al., "Room-Temperature  
10 Single-Electron Memory," IEEE Trans. Elec. Devices, Vol. 41, No. 9, pg. 1628 (September 1994), uses a tiny polysilicon strip which forms the source-to-drain path of the SEMM to store a discrete number of charges. An electron percolation path in the polysilicon strip forms the channel of the device, and one of the polysilicon grains next to the conduction path can act essentially in the same manner as a floating gate. However, because this structure relies  
15 on the polysilicon grain structure of the source-to-drain path as the storage medium, it inherently prevents a precise control of the channel size, the floating gate dimension, and the tunnel barrier.

In another previous SEMM design, disclosed in Sandip Tiwari, "A Silicon Nanocrystals Based Memory," App. Phys. Letters, Vol. 68, No. 10, pg. 1377 (March 1996), a  
20 conventional floating gate is replaced with a plurality of nanocrystal grains in a traditional floating gate memory. However, utilizing this approach, the size of the silicon nanocrystals

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forming the plurality of floating gates and the tunnel barriers associated with each floating gate will have an inherently broad distribution.

While both of these previous approaches strive to alleviate the challenges presented by nanofabrication (i.e., the fabrication of structures approaching the size of a nanometer), both rely on the use of statistically variant floating gate structures which lead to undesirable fluctuations in threshold voltage shifts and in the charging voltage, therefore making such structures unsuitable for large-scale integration. A commercially practical SEMM would require a voltage for charging a single electron to a floating gate to be discrete and well separated, and to result in a sufficient and predictable threshold voltage shift when a single electron is stored.

#### IV. SUMMARY OF THE INVENTION

The present invention provides a Single Electron MOS Memory (SEMM) capable of representing a bit of information (i.e., a logic '0' or a logic '1') by storing and detecting a single charge carrier during room temperature operation.

According to one aspect of the invention, the SEMM comprises a source-to-drain path with a channel region; a single floating gate for storing at least one charge carrier, the floating gate being disposed over the channel region and isolated from the channel region by a first gate dielectric layer; and a control gate disposed over the floating gate and isolated from the floating gate by a second gate dielectric layer so that the single charge carrier on the floating gate at room temperature produces a significant shift in threshold voltage of the channel region with respect to the control gate.

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According to another aspect of the invention, the SEMM comprises a semiconductor source-to-drain path which includes a channel region; a single floating gate disposed over the channel region and isolated from the channel region by a first gate dielectric layer, the floating gate having dimensions less than 10 nanometers (nm) by 10 nanometers by 10 nanometers for storing a single charge carrier; and a control gate disposed over the floating gate and isolated from the floating gate by a second gate dielectric layer. The width of the source-to-drain path is smaller than the Debye screening length of the single charge carrier stored on the floating gate.

According to another aspect of the invention, the SEMM comprises a source-to-drain path including a channel region having a width of less than 70 nanometers; a single floating gate disposed over the channel region and isolated from the channel region by a first gate dielectric layer, the floating gate having dimensions less than 10 nanometers by 10 nanometers by 10 nanometers for storing a single charge carrier; and a control gate disposed over the floating gate and isolated from the floating gate by a second gate dielectric layer.

According to another aspect of the invention, the SEMM comprises a source-to-drain path including a channel region between a source and a drain, the channel region being a semiconductor, the channel region having a length from the source to the drain and also having a width; a floating gate for storing at least one charge carrier, the floating gate being disposed over the channel region and isolated from the channel region by a first gate dielectric layer, the floating gate having a width, wherein the width of the floating gate is self-aligned with the width of the channel; and a control gate disposed over the floating gate and isolated from the floating gate by a second gate dielectric layer.

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According to another aspect of the invention, the SEMM comprises a source-to-drain path including a channel region between a source and a drain, the channel region being comprised of a semiconductor; a floating gate for storing at least one charge carrier, the floating gate being disposed over the channel region and isolated from the channel region by a first gate dielectric layer, the floating gate having lateral dimensions defined by lithography; and a control gate disposed over the floating gate and isolated from the floating gate by a second gate dielectric layer so that the single charge carrier on the floating gate at room temperature produces a significant shift in threshold voltage of the channel region with respect to the control gate.

According to another aspect of the invention, a method for fabricating a SEMM comprises forming a channel region of semiconductor material between a source and a drain, forming a first gate dielectric layer on the channel region, and forming a first conductor on the first gate dielectric layer to define a floating gate; oxidizing the floating gate to reduce its size; forming a second gate dielectric layer over the first conductor; and forming a second conductor over the second gate dielectric layer to define a control gate such that a single charge carrier stored on the floating gate produces a significant shift in the threshold voltage of the channel region with respect to the control gate.

According to another aspect of the invention, a method for fabricating a SEMM comprises forming a channel region of semiconductor material between a source and a drain; forming a first gate dielectric layer on the channel region; forming a first conductor on the first gate dielectric layer to define the floating gate; oxidizing the floating gate and the channel region to reduce their dimensions such that the resulting dimension of the floating

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gate is less than 10 nanometers by 10 nanometers by 10 nanometers, and such that the channel region has a width which is less than the Debye screening length of a single charge carrier stored on the floating gate; forming a second gate dielectric layer over the first conductor; and forming a second conductor over the second gate dielectric layer to define a control gate.

According to another aspect of the invention, a method for fabricating a SEMM on a substrate comprised of a buried dielectric layer with an overlying crystalline semiconductor layer comprises forming a first gate dielectric layer on the crystalline semiconductor layer; forming a first conductor on the first gate dielectric layer; etching the resulting structure to define the source-to-drain path of the storage device; etching a portion of the remaining first conductor to form a floating gate; forming a second gate dielectric layer on the floating gate; and forming a control gate on the second gate dielectric layer.

According to another aspect of the invention, a method for fabricating a SEMM is provided. The SEMM includes a source, a drain, a channel region having a length from the source to the drain and also having a width, a floating gate disposed over the channel region having a width, and a control gate disposed over the floating gate. The fabrication method comprises the steps of forming a first gate dielectric layer over a semiconductor material; forming a first conductor over the first gate dielectric; forming the channel region in the semiconductor material and forming the floating gate in the first conductor, wherein the width of the floating gate is self-aligned with the width of the channel; forming a second gate dielectric layer over the floating gate; and forming a second conductor over the second gate dielectric layer to define the control gate.

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According to another aspect of the invention, a method for fabricating a SEMM is provided. The SEMM includes a source, a drain, a channel region having a width between the source and the drain, a floating gate having a width and disposed over the channel region, the floating gate capable of storing a single charge carrier, and a control gate disposed over the floating gate. The fabrication method comprises the steps of forming a first gate dielectric over the channel region; forming the floating gate over the first gate dielectric wherein the lateral dimensions of the floating gate are defined by lithography; forming a second gate dielectric layer over the floating gate; and forming the control gate over the second gate dielectric layer, wherein the single charge carrier stored on the floating gate produces a significant shift in the threshold voltage of the channel region with respect to the control gate.

The SEMM of the invention solves the problems encountered with previous SEMM designs. The charging of the floating gate with a single charge carrier leads, at room temperature, to a quantized threshold voltage shift and a staircase relation between the shift and the charging voltage. Furthermore, the charging process is self-limited.

## V. BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a top-down view of the basic structure of a SEMM according to the present invention.

Figure 2 shows a cross-sectional view of the structure of Figure 1 along a source-to-drain path.

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Figure 3 shows an isometric view of a crystalline silicon substrate, a buried oxide layer, a surface layer, a gate oxide, and a first poly layer prior to a first lithographic step in the fabrication of the SEMM of Figure 1.

Figure 4 shows a cross-sectional view of the structure of Figure 3.

Figure 5 shows an isometric view of the structure of Figure 3 after the source-to-drain path is defined by the first lithographic step in the fabrication of the SEMM of Figure 1.

Figure 6 shows a cross-sectional view of the structure of Figure 5.

Figure 7 shows an isometric view of the structure of Figure 5 after the first poly layer is etched to form the floating gate.

Figure 8 shows a cross-sectional view of the structure of Figure 7 after the formation of thermal oxide and the deposition of additional oxide.

Figure 9 shows an isometric view of the structure of Figure 8 after the deposition of a second poly layer and the formation of the control gate from the second poly layer.

Figure 10 shows a cross-sectional view of the structure of Figure 9.

Figure 11 shows the I-V characteristics of the SEMM of Figure 1 after the application of several charging voltages.

Figure 12 shows the relationship between threshold voltage ( $V_t$ ) and charging voltage for the SEMM of Figure 1.

Figure 13 shows the relationship between threshold voltage ( $V_t$ ) and duration of charging pulse width for the SEMM of Figure 1.

Figure 14 shows an energy band diagram for the SEMM of Figure 1 showing charging of a single electron onto the floating gate.

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Figure 15 shows an energy band diagram for the SEMM of Figure 1 after a single electron has been charged onto the floating gate 26 and illustrates the Coulomb Blocking Effect by showing that the energy level inside of the floating gate 26 has been raised to prevent the charging of subsequent electrons.

5 Figure 16 shows a cross-sectional view of the SEMM of Figure 1 and shows the SEMM's inherent capacitances.

## VI. DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

Figures 1 and 2 show the disclosed inventive SEMM 10. The SEMM is comprised of:  
10 a crystalline silicon substrate 12; a buried oxide layer 14; a source-to-drain path 16 including a source 18, a drain 20, and a channel region 22; a gate oxide 24; a nanoscale floating gate or "dot" 26; a control gate oxide 28; and a control gate 30.

The SEMM's channel width 32 is narrower than the Debye screening length of a single electron stored on the floating gate 26. Therefore, the storage of a single electron on  
15 the floating gate 26 is sufficient to screen the entire channel (i.e., the full channel width 32) from the potential ( $V_{cg}$ ) on the floating gate. The storage of a single electron produces a significant shift in the SEMM's threshold voltage.

The small floating gate 26 significantly increases the quantum energy of the electron stored on the floating gate, a necessary constraint for room-temperature operation. At the  
20 same time, the small capacitance of the gate oxide 24 relative to the control gate oxide 28 allows for a sufficiently high charging voltage ( $V_{charge}$ ) such that the threshold voltage ( $V_t$ ) shift caused by an electron stored on the floating gate 26 and  $V_{charge}$  become well separated at

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room temperature. While the device's control gate 30 (and therefore the channel region 22) can be relatively long, the device's threshold voltage is determined by the section where the floating gate 26 is located over the channel region 22.

**A. Fabrication:**

5       The SEMM 10 can be fabricated using a silicon-on-insulator or SIMOX wafer 11 which comprises crystalline silicon 12 and a buried oxide layer 14. The buried oxide layer 14 is formed within the crystalline silicon 12 by high-energy ion implantation of oxygen, which leaves a 300-1000 nanometer thick surface layer 13 of crystalline silicon on top of the buried oxide layer 14. An anneal follows the ion implantation of oxygen to heal dislocations formed  
10   in the surface layer 13 as a result of the implantation. Depending on the implant energy used, the buried oxide layer 14 can be about 23 microns thick, although this thickness is not critical. A suitable wafer 11 pre-processed as described above can be purchased from IBIS, Inc., at 75 Arlington Street, Boston, Massachusetts, 02116. However, to tailor such a suitable wafer for use in fabricating the disclosed SEMM 10, it is necessary to thin the surface layer  
15   13 of crystalline silicon to about a 30-50 nanometers thickness. This can be performed by oxidizing the surface layer 13 in an oxygen ambient to consume as much of the surface layer 13 as necessary to achieve the proper thickness. The oxidized surface layer 13 is then removed by using a hydrofluoric acid wet etch. The surface layer 13 should be lightly doped to a concentration level of about  $1\text{E}14$  to  $1\text{E}19$  atoms/cm<sup>3</sup> (about  $4\text{E}14$  atoms/cm<sup>3</sup> is suitable)  
20   with a suitable P-type dopant such as boron. The surface layer 13 will eventually be etched to form the source-to-drain path 16, including the channel region 22, of the SEMM 10. While the use of a commercially available SIMOX wafer 11 is preferred, other Silicon on Insulator

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(SOI) technologies (such as Silicon on Sapphire (SOS) or mechanical bonding of crystalline silicon to a insulating substrate) are also suitable.

After removal of the excess surface layer 13, the gate oxide 24 is formed. For reasons to be clarified later, it is desirable to make the gate oxide very thin, on the order of about 1 nanometer. This can be achieved by exposing the etched surface layer 13 to an air ambient for about a day or two. The oxygen present in the air will react with the silicon in surface layer 13 to produce about 1 nanometer of oxide. Because this oxidation process is largely self-limiting, the exact time necessary to form the 1 nanometer is not critical.

Next, a first upodoped layer of polycrystalline silicon ("polysilicon" or "poly") 25 is deposited on top of the gate oxide 24 to a thickness of about 11 nanometers. The first poly layer 25 will eventually be patterned and etched to form the floating gate 26. The first poly layer 25 is preferably deposited using a Low-Pressure-Chemical-Vapor-Deposition (LPCVD) process which uses a silane ( $\text{SiH}_4$ ) source gas. Suitable poly LPCVD processes are well known to those of ordinary skill in the art. Figures 3 and 4 show the resulting structure after the completion of the above processing steps.

Next, the resulting structure is patterned and etched to form the source-to-drain path 16. Because the channel width 32 and the floating gate 26 must be very small, Electron Beam Lithography (EBL) is used during the patterning process. A suitable polymethymethacrylate (PMMA) resist (such as 950 K PMMA or other resist of a suitably low molecular weight) is deposited on the surface of the first poly layer 25 to a thickness of about 45 nanometers by spinning a 1.6% solution of PMMA (in chlorobenzine) at 6000 revolutions-per-minute for 60 seconds. The resulting structure is then baked for 12 hours at

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165 degrees Celsius to harden the PMMA resist. The PMMA resist is then exposed by an electron beam in the areas outside of the desired source-to-drain path 16 to degrade the PMMA so that it can be removed or "developed" in these areas. Development can be accomplished by rinsing the exposed resist at 23 degrees Celsius in 2-  
5 ethoxyethanol:methanol (3:7) for 7 seconds, followed by methanol for 10 seconds, followed by isopropanol for 30 seconds.

A suitable EBL system consists of a modified JEOL-840A Scanning Electron Microscope (SEM) with a tungsten filament gun which is equipped with a magnetic beam blanking unit and an electronic rotation system. Such a system is capable of producing a  
10 electron beam spot size of 3-4 nanometers and patterning a line width in the resist of about 20 nanometers.

During fabrication of the SEMM 10, this EBL system is used to pattern the source-to-drain path 16 to leave a line width of about 25 nanometers of resist in the channel region 22 of the device.

15 As an alternative to using EBL, nanoimprint technology can also be used to pattern the 25 nanometer line width. This technique involves making a mold containing the desired patterns to be etched and pressing it into the resist to leave an imprint of the pattern. Then, an etchant is used to etch the resist to expose the regions underneath the resist that that were recessed by the mold. Such a technique is disclosed in Stephen Y. Chou et al., "Imprint  
20 Lithography with 25-Nanometer Resolution," Science, Vol. 272, pg. 85 (April 5, 1996), which is incorporated into this application by reference in its entirety.

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Next, the resulting structure is anisotropically etched using Reactive-Ion-Etching (RIE) to etch the first poly layer 25, the gate oxide 24, and the surface layer 13. Etching is performed using a parallel plate RIE system operated at 13.56 MHz, with  $\text{Cl}_2$  and  $\text{SiCl}_4$  flow rates of 55 and 10 sccm, respectively, a power density of  $0.32 \text{ W/cm}^2$ , a pressure of 40 mTorr, and a self-bias of -85 Volts. This produces a silicon etch rate of about 150 nanometers/minute. While the etching process as disclosed will etch silicon (i.e., the first poly layer 25 and the surface layer 13) at least ten times faster than oxides (i.e., the gate oxide 24), the process can also be used to remove the very thin layer of gate oxide 24. The etch time merely needs to be adjusted to account for the extra time needed to etch through the gate oxide 24. Also, the etching process as disclosed will etch silicon (i.e., the first poly layer 25 and the surface layer 13) at least ten times faster than the PMMA resist. Thus, using the thicknesses disclosed, a sufficient amount of PMMA will be left over the source-drain path 16 and will protect the underlying first poly layer 25 from being inadvertently etched. After etching, the PMMA resist can be removed by first soaking the resulting structure in warm acetone and later spraying the structure with a pressurized acetone jet. Because the first poly layer 25 and the channel region 22 are etched using the same photoresist mask, the width of the floating gate 26 (to be formed from the first poly layer 25) and the width of channel region 22 (formed from surface layer 13) are self-aligned with respect to one another. Figures 5 and 6 show the resulting structure after the completion of the above processing steps.

Next, the floating gate 26 is formed from the remaining first poly layer 25. This can be accomplished by using the same patterning and etching steps that were used to form the source-to-drain path 16 as described above, except that the poly etch time needs to be

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adjusted to stop the etch after the gate oxide 24 surface has been reached. After the etch, the lateral area of the floating gate 26 will be about 25 nanometers by 25 nanometers. Figure 7 shows the resulting structure after the completion of the above processing steps.

After the floating gate 26 has been etched and the PMMA resist removed, the  
5 resulting structure is then oxidized preferably in an ambient containing 100% oxygen for about 12 minutes at 900 degrees Celsius, atmospheric pressure, to form thermal oxide 27. The purpose of this oxidation step is three-fold: first, the high temperature of the oxidation process helps to anneal any damage to the surface layer 13 that might have resulted from the previous etching steps; second, the oxidation of the floating gate 26 will cause the polysilicon  
10 in the floating gate to oxidize, thus reducing its size to suitably quantize the energy levels of a single charge carrier on the floating gate; and third, the oxidation on the top of the floating gate 26 comprises a portion of the control gate oxide 28 (to be described in more detail later). The oxidation step should consume about 9 nanometers from each of the exposed surfaces of the 25 nanometers by 25 nanometers by 11 nanometers patterned floating gate 26, thus  
15 reducing its size after oxidation to about 7 nanometers by 7 nanometers by 2 nanometers. Of course, one of ordinary skill will recognize that self-limiting oxidation, as discussed in H.I. Liu et al, "Self-Limiting Oxidation for Fabricating sub-5 nm Silicon Nanowires," Applied Physics Letters, Vol. 64, pg. 1383 (1994), makes it difficult to assess the exact size of the resulting floating gate 26. The channel region 22 will also be oxidized by this process,  
20 although at a slightly slower rate than the floating gate 26, achieving a final channel width 32 of about 10 nanometers. Because the oxidation of silicon will form a resulting oxide film

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which is about twice the thickness of the silicon consumed by the oxidation, the thermal oxide 27 on the top and sides of the floating gate will be about 18 nanometers thick.

While the oxidation times, temperatures, gas concentrations, and gas flow rates as disclosed achieve the goals of fabricating a sufficiently small floating gate 26 and annealing prior etching damage, these parameters can be modified if necessary. For example, if longer heat treatments are needed to heal etch damage than are required to oxidize the floating gate, nitrogen can be added to the oxygen ambient to retard oxidation.

Next, an oxide 29 is deposited on the resulting structure to a thickness of 22 nanometers using a commercially available Plasma-Enhanced-Chemical-Vapor-Deposition (PECVD) system. Oxide 29, when combined with the 18 nanometers of thermal oxide 27 already present on the top and sides of the floating gate 26 as a result of the previous oxidation step, produces a control gate oxide 28 which is about 40 nanometers thick. Figure 8 shows the resulting structure after the completion of the above processing steps.

Next, a second undoped layer of poly 31 is deposited on top of the control gate oxide 28. The thickness of the second poly layer 31 is not critical and can be, for example, 100 to 500 nanometers thick. Otherwise, the second poly layer 31 is deposited using the same process used to deposit the first poly layer 25. The second poly layer 31 is then patterned and etched to form the control gate 30. Because the lateral dimensions of control gate 26 can be relatively large (e.g., about 1 to 3 microns), it can be patterned with optical lithography processes currently in use in the production of modern-day semiconductor circuits. Such optical lithography processes are easily capable of patterning resist line widths of less than a micron and are well known to those of ordinary skill in the art. After patterning, the second

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poly layer 31 can be etched using the poly etch recipe disclosed above, with the etch time adjusted to account for the extra thickness of the second poly layer 31. The length of the control gate will ultimately define the extent of the channel region 22 of the SEMM device. Also, the width of the control gate 30 is not critical, but is preferably made to run over the  
5 sides of the floating gate 26.

Next, the resulting structure is ion implanted with arsenic (an N-type dopant) to dope the exposed regions of the source-to-drain path 16 and the control gate 30. This doping step has a two-fold purpose; first, it dopes the control gate 30 to render it sufficiently conductive to carry signals without undue resistance; and second, it dopes the exposed portions of the  
10 source-to-drain path 16 in those regions not covered by the control gate 30 to form source 18 and drain 20. The resulting undoped region of the source-to-drain path 16 (i.e., the region "masked" by the control gate 30) constitutes the channel region 22 of the device. While the exact doping concentration to be achieved is not critical, a high doping concentration of about  $10^{19}$  arsenic atoms/cm<sup>3</sup> is sufficient to render the exposed portions of the source-to-drain path  
15 16 and the control gate 30 sufficiently conductive. Note that the existence of the thin gate oxide 24 will not appreciably affect the implantation of the exposed portions of the source-to-drain path 16. Figures 9 and 10 show the resulting structure after the completion of the above processing steps.

The subsequent processing steps necessary to complete the manufacture of the SEMM  
20 10 can be performed using industry standard techniques well known to those of ordinary skill in the art of semiconductor processing and therefore are only briefly described and not shown in the Figures. An interlevel dielectric such as an oxide is deposited over the surface of the

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resulting structure. Next, holes are etched through the interlevel dielectric and other oxides present to expose a portion of the source 18, the drain 20, and the control gate 30 of the SEMM 10. Next, a conductive layer (preferably aluminum) is sputtered onto the surface of the resulting structure such that the conductive layer comes into electrical contact with the source 18, drain 20, and control gate 30 through the contact holes. The conductive layer is then sintered in an inert forming gas of 30% hydrogen-70% nitrogen at 400 degrees Celsius for about 20 minutes. The purposes of the sintering process are two fold: first, it causes the metal to diffuse into and alloy with the silicon in the source 18, drain 20, and control gate 30 to provide a suitably low-resistance contact to these regions; and second, it removes any interface states present at the gate oxide 24/channel region 22 interface, thus providing more stable electrical operation of the SEMM device. Thereafter, the metal can be patterned and etched to produce leads connected to the source 18, drain 20, and control gate 30 contacts. Then a suitable passivating layer (such as an oxide or nitride) can be deposited over the resulting structure with holes etched therethrough to receive the signals necessary to operate the device (e.g., from bonding wires or probe tips).

#### **B. Characterization/Experimental Results:**

A batch of about thirty SEMM devices were fabricated as described above using the modified electron microscope for EBL. These SEMM devices were characterized at room temperature using a two-step process. First, a positive voltage pulse (i.e., a charging voltage,  $V_{\text{charge}}$ ) relative to the grounded source was applied to the control gate 30, while the drain voltage was maintained at 50 mV (millivolts). This process causes electrons to tunnel from the channel region 22 to the floating gate 26. Second, the I-V characteristics of the SEMM

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10 were measured by monitoring the source-to-drain current ( $I_{ds}$ ) flowing through the source-to-drain path 16 as a function of control gate voltage ( $V_{cg}$ ), using a 50 mV source-to-drain voltage. The I-V characteristics reveal the threshold voltage ( $V_t$ ) of the device, defined as the  $V_{cg}$  value at which  $I_{ds} = 100$  pA. A simple switching circuit was used to allow I-V  
5 measurements to be taken within 1 second after the charging process was completed.

A SEMM 10 having a channel width 32 of about 10 nanometers and a floating gate 26 with dimensions 7 nanometers by 7 nanometers by 2 nanometers (the smallest device fabricated) was characterized after the application of different charging voltages. Figure 11 shows the I-V characteristics of the device after the control gate 30 was pulsed for 10 ms with  
10 charging voltages ( $V_{charge}$ ) of 2V, 7V, 10V and 14V. Note that as  $V_{charge}$  is increased, the  $V_t$  of the SEMM 10 increases by discrete steps of about 55 mV. Figure 12 shows this same data in a different form, plotting  $V_t$  versus  $V_{charge}$ . The 55 mV shifts can also be seen in Figure 12, and discrete 55 mV shifts are seen when  $V_{charge}$  increases by about 4 Volts. Figure 13 shows that, for a given  $V_{charge}$  (i.e., 10V), the  $V_t$  shift is self-limited and is independent of the  
15 charging time (i.e., the  $V_{charge}$  pulse width). This data shows that a discrete number of electrons (e.g., one when  $V_{charge} = 5$  to 8 Volts; two when  $V_{charge} = 9$  to 12 V; and three when  $V_{charge} = 13$  or greater) are stored on the floating gate 26. These electrons will tunnel back into the channel within about 5 seconds after the charging voltage is removed, although this phenomenon can be curtailed by increasing the thickness of the gate oxide 24.

20 Despite the extremely small floating gate 26 and the very low channel region 22 doping concentration, Figure 11 shows that the disclosed SEMM 10 has a good subthreshold slope of 108 mV/decade. This results because the inversion layer induced by the control gate

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effectively acts as an ultra shallow source and drain for the SEMM 10, and also because the source-to-drain voltage is low.

It is noted that the discrete threshold shift is not due to interfacial traps at the gate oxide 24/channel region 22 interface. The threshold shifts due to these traps cannot provide  
5 equally spaced threshold shifts because the charges will be trapped at different locations in the channel. Furthermore, the charging of interface traps is known to be time dependent, *see e.g.* J.R. Davis, "Instabilities in MOS Devices," Gordon & Breach Science Publishers (1980), a characteristic not present in the experimental data (see Figure 13).

#### 1. The $V_t$ v. Charging Voltage "Staircase" Function:

10 In the fabricated batch of SEMMs, no gate oxide was intentionally grown or deposited over the native oxide between the channel region 22 and floating gate 26, resulting in a very thin gate oxide 24. The reasons were two-fold: to allow fast charging of an electron onto the floating gate 26; and to minimize the potential difference between the channel region 22 and the floating gate 26 during the charging process. Minimization of the potential difference  
15 between the channel region 22 and the floating gate 26 allows the SEMM 10 to exploit a phenomenon known as the Coulomb Blockade Effect.

In the Coulomb Blocking Effect, when a relatively high  $V_{\text{charge}}$  (e.g., 5 to 8 Volts) is present on the control gate, an electron in the channel region 22 can tunnel through the gate oxide 24 and come to rest on the floating gate 26. The presence of the electron on the  
20 floating gate perturbs the electric field provided by  $V_{\text{charge}}$  such that further electrons will not have an incentive to tunnel through the gate oxide 24. This is illustrated by the energy band diagrams of Figures 14 and 15. Figure 14 shows the energy band diagram of the SEMM 10

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when the floating gate 26 is being charged with an electron. Figure 15 shows how the stored electron perturbs the electric field within the gate oxide 24, through which the electron must tunnel to reach the floating gate 24. Specifically, a stored electron will raise the energy level of the floating gate 26 by  $q^2/C_{it}$ , where  $q$  = electron charge =  $1.6 \times 10^{-19}$  Coulombs, and  $C_{it}$  = the total capacitance of the floating gate  $\approx C_{dc}$ , where  $C_{dc}$  is the capacitance from the floating gate (or "dot") 26 to the channel region 22. (See Figure 16 for a diagram of the capacitances inherent within the SEMM 10 that are helpful in understanding its operation). Therefore, the stored electron effectively screens the charging voltage  $V_{charge}$  and prevents the formation of a tunneling field within the gate oxide 24, and thus a single electron can be stored onto the floating gate 26. Of course, the Coulomb Blockade Effect and the screening effect of the stored electron can be overcome by the addition of a higher  $V_{charge}$  (e.g., 9-12V), which would then allow a second electron to tunnel onto the floating gate, as proven by the experimental data. Further increases in  $V_{charge}$  (e.g., 13 V or greater) will overcome the screening effect of the two electrons to permit a third electron to tunnel onto the floating gate, and so on.

Because the gate oxide 24 is much thinner than the control gate oxide 28, almost all of the charging voltage  $V_{charge}$  will be dropped across the control gate oxide 28. This means that, to add a single electron to the floating gate 26, a  $V_{charge} = q/C_{dg}$  is required, where  $C_{dg}$  is the capacitance between the control gate and the floating gate (Figure 12).  $C_{dg}$  for a 7 nanometer by 7 nanometer floating gate with 40 nanometers of control oxide is about  $4.4 \times 10^{-20}$  Farads, and therefore  $q/C_{dg} = 3.6V$ , which is close to the experimental  $V_{charge} = 4$  to 5 Volts.

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## 2. The Discrete 55 mV $V_t$ Shift:

The shift in the SEMM's threshold voltage when one electron is stored on the floating gate 26 is governed by the equation:  $\Delta V_t \approx q/(C_{dg} + C_{frg})$ , where  $C_{frg}$  is the fringe capacitance resulting from the wrapping of the control gate 30 around the channel region 22, such that the channel region 22 is only partially screened by the floating gate 26. For a conventional floating gate MOS memory,  $C_{frg} \approx 0$ , and  $\Delta V_t \approx q/C_{dg}$ . In the disclosed SEMM 10,  $C_{frg}$  is about two orders of magnitude greater than  $C_{dg}$ , and can be estimated using a single-electron Debye screen length (about 70 nanometers; see below for a detailed discussion) and the channel thickness (about 26 nanometers) using a parallel-plate capacitor model. Accordingly, for a control gate oxide 28 thickness of 40 nanometers and an area of 70 x 26 x 2 nanometers squared,  $C_{frg}$  is about  $2.5 \cdot 10^{-18}$  Farads, and  $\Delta V_t \approx 64$  mV, which is consistent with the experimental value 55 mV shown in Figures 11 and 12.

As indicated by the equation shown above, the threshold voltage can be adjusted to be larger than 55 mV by increasing the control gate oxide 28 thickness to reduce  $C_{dg}$ , or by reducing  $C_{frg}$ .

Also, it should be noted that the 55 mV  $V_t$  shift produced is significant and sufficiently distinct from expected thermal variations, therefore ensuring the reliability of exploiting the shift to produce effective memory cells. At room temperature, thermal variations will be on the order of  $kT/q$ , where  $T = 300$  Kelvin, and  $k =$  Boltzmann constant =  $8.62 \cdot 10^{-5}$  electron Volts/degree Kelvin, and  $q =$  electron charge =  $1.6 \cdot 10^{-19}$  Coulombs. This value at room temperature is about 26 mV, which is comfortably less than the 55 mV  $V_t$  shift.

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### 3. Operational Physics:

Critical to the operation of the SEMM is the manufacture of the nanoscale floating gate 26. When the floating gate 26 is made sufficiently small, the energy levels within the floating gate 26 become quantized and separate. By further reducing the size of the floating gate 26, the energy spacing between these quantum levels becomes sufficiently large. Because the energy spacings are dictated by quantum mechanics and the solution of the Schrödinger Equation, it is difficult to quantify the exact floating gate 26 size that will produce a sufficient energy spacing within the floating gate 26. However, if the floating gate 26 is approximated to be a spherical "dot" with radius  $r$ , the energy spacing inside the dot is determined by the solution of the Schrödinger Equation. As a first order approximation, if the floating gate 26 is assumed to be a substantially flat "disk" of radius  $r$ , solutions to the Schrödinger Equation show that the energy level spacings within the floating gate "dot" are proportional to  $1/r^2$ . Solutions to the Schrödinger Equation are outlined in Stephen Gasiorowicz, "Quantum Physics," John Wiley & Sons, pp. 60-64, 78-79, 151-152 (1974), which is incorporated herein by reference in its entirety. Of course, as previously noted in section IV(B)(1) above, the energy levels in the floating gate "dot" are also a function of the coulomb charging energy  $= q^2/C_{tt}$ . Because  $C_{tt}$  varies roughly linearly with  $r$  for thin dielectrics approaching the radius of the "dot," the coulomb charging energy is roughly proportional to  $1/r$ . Thus, at very small radii  $r$ , the quantum mechanical effects will dominate over coulomb charging effects.

Increasing the quantum energy level spacing within the floating gate 26 is important, because, for room temperature operation (i.e., about 300 degrees Kelvin), the quantum energy

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level spacing within the floating gate 26 must be significantly higher than the thermal energy of an electron, i.e., 26 mV. If not, a sufficiently "hot" electron will be able to overcome the energy barrier and appear on the floating gate, without the assistance and control of the charging voltage. This situation precludes the ability of storing a single electron in a controlled manner.

Using a SEMM 10 fabricated in the disclosed manner, the estimated quantum energy level spacing in the disclosed floating gate 26 is about 80 meV, or about 3 times the thermal energy of an electron at room temperature.

It is also critical to the operation of the device that a single electron stored on the floating gate 26 be able to modulate the conductivity of the channel such that a resolvable shift in  $V_t$  results. More specifically, the channel width 32 must generally be smaller than the Debye screening length of a single electron stored on the floating gate 26. The Debye screening length,  $L_D$  for the disclosed SEMM 10 is estimated to be about 70 nanometers, and is governed by the following equation:

$$L_D = \sqrt{(\epsilon_s kT / q^2 N_B)}$$

where  $\epsilon_s$  = permittivity of silicon ( $11.9 * 8.85E-14$  Farads/cm),  $k$  = Boltzmann constant,  $T$  = temperature (e.g., 300 degrees Kelvin),  $q$  = electron charge, and  $N_B$  = doping of the channel region 22 (e.g.,  $4E14$  boron atoms/cm<sup>3</sup>). Of course, this equation provides a simplified model and one of ordinary skill will realize that the Debye screening length in an operational device will vary from this ideal value, and may need to be experimentally determined. Because the channel width 32 of the disclosed SEMM 10 after oxidation is about 10 nanometers, a single

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electron can effectively modulate the channel conductivity, even when the control gate 30 is allowed to overlap the sides of the channel region 22. Furthermore, because the Debye screening length is much larger than the disclosed channel width 32, a SEMM device should be functional even when larger channel widths 32 are used, although the self-aligned structure  
5 of the SEMM 10 as disclosed assures that the channel width 32 is sufficiently small. As disclosed, the stored electron (or electrons) modulate the channel by causing the positive charges in the p-doped channel to be attracted to the gate oxide 24/channel region 22 interface. This in turn makes it more difficult for the voltage on the control gate ( $V_{cg}$ ) to invert the channel region 22 to produce a sufficient source-to-drain current ( $I_{ds}$ ) in the channel  
10 region 22 of the source-to-drain path 16, thus increasing the SEMM's  $V_t$  (i.e., by 55 mV).

### C. Conclusion:

A SEMM according to the invention has been shown useful for storing and detecting the presence of single electrons at room temperature. The SEMM is orders of magnitude  
15 smaller than conventional floating gate memories, has unique properties that conventional memories do not have, and constitutes a major step towards utilizing single electron effects to build ultra-small and ultra-high density transistor memories.

Those of ordinary skill in the art who now have the benefit of the present disclosure will appreciate that the present invention may take many forms and embodiments and have  
20 many uses. Moreover, those of ordinary skill will realize that the manufacturing details as set forth are merely one way of fabricating the SEMM, and that many other ways are possible which do not depart from the invention disclosed herein. For example, many different

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materials may be used in the fabrication of a SEMM of the present invention. Thus, the various dielectrics such as gate oxide 24 and control gate oxide 28 could also be formed of silicon nitride, tantalum dioxide or other suitable dielectric materials, or combinations thereof. Also, the floating gate could be formed of other suitably conductive materials, such as various metallic silicides (such as tungsten or titanium silicide). Other minor changes to the process are also possible without departing from the invention in any significant respect.

Accordingly, it is intended that the embodiments described herein should be illustrative only, and not limiting with respect to the scope of the present invention. Rather, it is intended that the invention encompass all modifications, equivalents and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

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**WHAT IS CLAIMED IS:**

1. A data storage device, comprising:
  - (a) a source-to-drain path including a channel region between a source and a drain, the channel region being comprised of a semiconductor;
  - 5 (b) a single floating gate for storing at least one charge carrier, the floating gate being disposed over the channel region and isolated from the channel region by a first gate dielectric layer; and
  - (c) a control gate disposed over the floating gate and isolated from the floating gate by a second gate dielectric layer so that the single charge carrier on the floating gate  
10 at room temperature produces a significant shift in threshold voltage of the channel region with respect to the control gate.
2. The data storage device of claim 1, wherein the charge carrier is an electron.
3. The data storage device of claim 1, wherein the shift in the threshold voltage is greater than 26 millivolts at room temperature.
- 15 4. The data storage device of claim 1, wherein the single floating gate has dimensions less than 10 nanometers by 10 nanometers by 10 nanometers.
5. The data storage device of claim 1, wherein the single floating gate has dimensions less than 30 nanometers by 30 nanometers by 30 nanometers.
6. The data storage device of claim 1, wherein the channel region has a width of less  
20 than 70 nanometers.

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7. The data storage device of claim 1, wherein the semiconductor is crystalline silicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

8. The data storage device of claim 1, wherein the semiconductor is crystalline silicon, the floating gate is polysilicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

9. The data storage device of claim 1, wherein the first gate dielectric layer has a thickness of about 1 nanometer.

10. A data storage device, comprising:

10 (a) a source-to-drain path including a channel region between a source and a drain, the channel region being comprised of a semiconductor;

(b) a single floating gate disposed over the channel region and isolated from the channel region by a first gate dielectric layer, the floating gate having dimensions less than 10 nanometers by 10 nanometers by 10 nanometers for storing a single charge carrier; and

15 (c) a control gate disposed over the floating gate and isolated from the floating gate by a second gate dielectric layer;

wherein the channel region has a width smaller than a Debye screening length of the single charge carrier stored on the floating gate.

20 11. The data storage device of claim 10, wherein the charge carrier is an electron.

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12. The data storage device of claim 10, wherein storage of the single charge carrier on the floating gate causes a shift in threshold voltage of the channel region with respect to the control gate of greater than 26 millivolts at room temperature.

13. The data storage device of claim 10, wherein the channel region has a width of less  
5 than 70 nanometers.

14. The data storage device of claim 10, wherein the semiconductor is crystalline silicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

15. The data storage device of claim 10, wherein the semiconductor is crystalline silicon,  
10 the floating gate is polysilicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

16. The data storage device of claim 10, wherein the first gate dielectric layer has a thickness of about 1 nanometer.

17. A storage device, comprising:

15 (a) a source-to-drain path including a channel region between a source and a drain, the channel region being comprised of a semiconductor, the channel region having a width of less than 70 nanometers;

(b) a single floating gate disposed over the channel region and isolated from the channel region by a first gate dielectric layer, the floating gate having dimensions  
20 less than 10 nanometers by 10 nanometers by 10 nanometers for storing a single charge carrier; and

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(c) a control gate disposed over the floating gate and isolated from the floating gate by a second gate dielectric layer.

18. The storage device of claim 17, wherein the charge carrier is an electron.

19. The storage device of claim 17, wherein storage of the single charge carrier on the floating gate causes a shift in threshold voltage of the channel region with respect to the control gate of greater than 26 millivolts at room temperature.

20. The storage device of claim 17, wherein the semiconductor is crystalline silicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

21. The storage device of claim 17, wherein the semiconductor is crystalline silicon, the floating gate is polysilicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

22. The storage device of claim 17, wherein the first gate dielectric layer has a thickness of about 1 nanometer.

23. A data storage device, comprising:

(a) a source-to-drain path including a channel region between a source and a drain, the channel region being a semiconductor, the channel region having a length from the source to the drain and also having a width;

(b) a floating gate for storing at least one charge carrier, the floating gate being disposed over the channel region and isolated from the channel region by a first gate dielectric layer, the floating gate having a width, wherein the width of the floating gate is self-aligned with the width of the channel; and

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(c) a control gate disposed over the floating gate and isolated from the floating gate by a second gate dielectric layer.

24. The data storage device of claim 23, wherein the single charge carrier on the floating gate at room temperature produces a significant shift in threshold voltage of the channel region with respect to the control gate.

25. The data storage device of claim 24, wherein the significant shift in threshold voltage is greater than or equal to about 26 mV.

26. The data storage device of claim 23, wherein the floating gate is self-aligned with the width of the channel by simultaneously patterning and etching the floating gate and the semiconductor to define the width of the floating gate and the width of the channel region respectively.

27. The data storage device of claim 23, wherein the width of the channel region is smaller than a Debye screening length of the single charge carrier stored on the floating gate.

28. The data storage device of claim 23, wherein the charge carrier is an electron.

29. The data storage device of claim 23, wherein the floating gate has dimensions less than 10 nanometers by 10 nanometers by 10 nanometers.

30. The data storage device of claim 23, wherein the floating gate has dimensions less than 10 nanometers by 10 nanometers by 10 nanometers.

31. The data storage device of claim 23, wherein the semiconductor is crystalline silicon, the floating gate is polysilicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

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32. The data storage device of claim 23, wherein the semiconductor is crystalline silicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

33. The data storage device of claim 23, wherein the first gate dielectric layer has a  
5 thickness of about 1 nanometer.

34. A data storage device, comprising:

(a) a source-to-drain path including a channel region between a source and a drain, the  
channel region being comprised of a semiconductor;

(b) a floating gate for storing at least one charge carrier, the floating gate being  
10 disposed over the channel region and isolated from the channel region by a first  
gate dielectric layer, the floating gate having lateral dimensions defined by  
lithography; and

(c) a control gate disposed over the floating gate and isolated from the floating gate by  
a second gate dielectric layer so that the single charge carrier on the floating gate  
15 at room temperature produces a significant shift in threshold voltage of the  
channel region with respect to the control gate.

35. The data storage device of claim 34, wherein the charge carrier is an electron.

36. The data storage device of claim 34, wherein the shift in the threshold voltage is  
greater than 26 millivolts at room temperature.

20 37. The data storage device of claim 34, wherein the single floating gate has dimensions  
less than 10 nanometers by 10 nanometers by 10 nanometers.

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38. The data storage device of claim 34, wherein the single floating gate has dimensions less than 30 nanometers by 30 nanometers by 30 nanometers.

39. The data storage device of claim 34, wherein the channel region has a width of less than 70 nanometers.

40. The data storage device of claim 34, wherein the semiconductor is crystalline silicon, the floating gate is polysilicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

41. The data storage device of claim 34, wherein the semiconductor is crystalline silicon, the floating gate is polysilicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

42. The data storage device of claim 34, wherein the first gate dielectric layer has a thickness of about 1 nanometer.

43. A method for producing a data storage device, the method comprising the steps of:

(a) forming a channel region of semiconductor material between a source and a drain,

forming a first gate dielectric layer on the channel region, and forming a first conductor on the first gate dielectric layer to define a floating gate;

(b) oxidizing the floating gate to reduce its size;

(c) forming a second gate dielectric layer over the first conductor; and

(d) forming a second conductor over the second gate dielectric layer to define a control gate,

wherein a single charge carrier stored on the floating gate produces a significant shift in the threshold voltage of the channel region with respect to the control gate.

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44. The method of claim 43, wherein the charge carrier is an electron.

45. The method of claim 43, wherein the shift in the threshold voltage is greater than 26 millivolts at room temperature.

46. The method of claim 43, wherein the width of the channel region and the width of the floating gate are defined by one lithography patterning step so that the width of the floating gate is self-aligned with the width of the channel region.

47. The method of claim 43, wherein the semiconductor material is crystalline silicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

48. The method of claim 43, wherein the semiconductor material is crystalline silicon, the floating gate is polysilicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

49. The method of claim 43, wherein the single floating gate has dimensions less than 10 nanometers by 10 nanometers by 10 nanometers after the floating gate is oxidized to reduce its size.

50. The method of claim 43, wherein the single floating gate has dimensions less than 30 nanometers by 30 nanometers by 30 nanometers after the floating gate is oxidized to reduce its size.

51. The method of claim 43, wherein the single floating gate has dimensions less than 10 nanometers by 10 nanometers by 10 nanometers after the floating gate is oxidized to reduce its size, and greater than 10 nanometers by 10 nanometers by 10 nanometers before the floating gate is oxidized to reduce its size.

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52. The method of claim 43, wherein the channel region has a width of less than 70 nanometers.

53. The method of claim 43, wherein the first gate dielectric layer has a thickness of about 1 nanometer.

5 54. The method of claim 43, further comprising oxidizing the channel region to reduce its width.

55. A method for producing a data storage device, the method comprising the steps of:

(a) forming a channel region of semiconductor material between a source and a drain,

forming a first gate dielectric layer on the channel region, and forming a first

10 conductor on the first gate dielectric layer to define the floating gate;

(b) oxidizing the floating gate and the channel region to reduce their dimensions such

that the resulting dimension of the floating gate is less than 10 nanometers by 10

nanometers by 10 nanometers, and such that the channel region has a width which

is less than the Debye screening length of the single charge carrier which is stored

15 on the floating gate;

(c) forming a second gate dielectric layer over the first conductor; and

(d) forming a second conductor over the second gate dielectric layer to define a

control gate.

56. The method of claim 55, wherein the charge carrier is an electron.

20 57. The method of claim 55, wherein the shift in the threshold voltage is greater than 26 millivolts at room temperature.

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58. The method of claim 55, wherein the width of the channel region and the width of the floating gate are defined by one lithography patterning step so that the width of the floating gate is self-aligned with the width of the channel region.

59. The method of claim 55, wherein the semiconductor material is crystalline silicon, the floating gate is polysilicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

60. The method of claim 55, wherein the semiconductor material is crystalline silicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

61. The method of claim 55, wherein the single floating gate has dimensions greater than 10 nanometers by 10 nanometers by 10 nanometers before the floating gate is oxidized to reduce its dimension.

62. The method of claim 55, wherein the channel region has a width of less than 70 nanometers.

63. The method of claim 55, wherein the first gate dielectric layer has a thickness of about 1 nanometer.

64. The method of claim 55, further comprising oxidizing the channel region to reduce its width.

65. A method for producing a data storage device on a substrate comprised of a buried dielectric layer and a crystalline semiconductor layer disposed over the buried dielectric layer, the method comprising the steps of:

(a) forming a first gate dielectric layer on the crystalline semiconductor layer;

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- (b) forming a first conductor on the first gate dielectric layer;
- (c) etching the resulting structure to remove a portion of the first conductor, the first gate dielectric layer, and the crystalline semiconductor layer, thereby defining a strip comprised of the remaining first conductor, the first gate dielectric layer, and the crystalline semiconductor layer, the remaining crystalline semiconductor layer defining the source-to-drain path of the storage device;
- (d) etching a portion of the remaining first conductor of the strip to form a floating gate;
- (e) forming a second gate dielectric layer on the floating gate; and
- (f) forming a control gate on the second gate dielectric layer.

66. The method of claim 65, wherein in step (c) the first conductor, the first gate dielectric layer, and the crystalline semiconductor material are etched in a manner to self-align the remaining first conductor with the remaining crystalline semiconductor material.

67. The method of claim 65, further comprising, after step (d), oxidizing the floating gate and the remaining crystalline semiconductor to narrow the size of the floating gate and the width of source-to-drain path.

68. The method of claim 67, wherein, after oxidation, the floating gate has dimensions of less than 10 nanometers by 10 nanometers by 10 nanometers.

69. The method of claim 67, wherein, after oxidation, the floating gate has dimensions of less than 30 nanometers by 30 nanometers by 30 nanometers.

70. The method of claim 65, wherein the width of the source-to-drain path is smaller than the Debye screening length of a single charge carrier to be stored on the floating gate.

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71. The method of claim 65, wherein the semiconductor material is crystalline silicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

72. The method of claim 65, wherein the semiconductor material is crystalline silicon, the floating gate is polysilicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

73. The method of claim 65, wherein the buried dielectric layer is a buried oxide layer and is formed by ion implanting oxygen into the substrate.

74. A method for producing a data storage device, the storage device including a source, a drain, a channel region having a length from the source to the drain and also having a width, a floating gate disposed over the channel region having a width, and a control gate disposed over the floating gate, the method comprising the steps of:

(a) forming a first gate dielectric layer over a semiconductor material;

(b) forming a first conductor over the first gate dielectric;

(c) forming the channel region in the semiconductor material and forming the floating gate in the first conductor, wherein the width of the floating gate is self-aligned with the width of the channel;

(d) forming a second gate dielectric layer over the floating gate; and

(e) forming a second conductor over the second gate dielectric layer to define the control gate.

75. The method of claim 74, wherein the floating gate is oxidized to reduce its size.

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76. The method of claim 75, wherein the floating gate has dimensions less than 10 nanometers by 10 nanometers by 10 nanometers after the floating gate is oxidized to reduce its size.

77. The method of claim 75, wherein the floating gate has dimensions less than 30 nanometers by 30 nanometers by 30 nanometers after the floating gate is oxidized to reduce its size.

78. The method of claim 75, wherein the floating gate has dimensions less than 10 nanometers by 10 nanometers by 10 nanometers after the floating gate is oxidized to reduce its size, and greater than 10 nanometers by 10 nanometers by 10 nanometers before the floating gate is oxidized to reduce its size.

79. The method of claim 74, wherein a single charge carrier stored on the floating gate produces a significant shift in the threshold voltage of the channel region with respect to the control gate.

80. The method of claim 79, wherein the charge carrier is an electron.

81. The method of claim 79, wherein the shift in the threshold voltage is greater than 26 millivolts at room temperature.

82. The method of claim 74, wherein the width of the channel region and the width of the floating gate are self-aligned by one lithography patterning and etching step.

83. The method of claim 74, wherein the semiconductor material is crystalline silicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

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84. The method of claim 74, wherein the semiconductor material is crystalline silicon, the floating gate is polysilicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

85. The method of claim 74, wherein the channel region has a width of less than 70

5 nanometers.

86. The method of claim 74, wherein the first gate dielectric layer has a thickness of about 1 nanometer.

87. A method for producing a data storage device, the storage device including a source, a drain, a channel region having a width between the source and the drain, a floating gate

10 having a width and disposed over the channel region, the floating gate capable of storing a single charge carrier, and a control gate disposed over the floating gate, the method comprising the steps of:

(a) forming a first gate dielectric over the channel region;

(b) forming the floating gate over the first gate dielectric wherein the lateral

15 dimensions of the floating gate are defined by lithography;

(c) forming a second gate dielectric layer over the floating gate; and

(d) forming the control gate over the second gate dielectric layer,

wherein the single charge carrier stored on the floating gate produces a significant

shift in the threshold voltage of the channel region with respect to the control gate.

20 88. The method of claim 87, wherein the charge carrier is an electron.

89. The method of claim 87, wherein the shift in the threshold voltage is greater than 26 millivolts at room temperature.

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90. The method of claim 87, wherein the width of the channel region and the width of the floating gate are defined by one lithography patterning step so that the floating gate is self-aligned with the channel region.

91. The method of claim 87, wherein the floating gate is polysilicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

92. The method of claim 87, wherein the floating gate is polysilicon, the first gate dielectric layer includes an oxide of silicon, and the second gate dielectric layer includes an oxide of silicon.

93. The method of claim 87, comprising the further step of oxidizing the floating gate to reduce its size.

94. The method of claim 93, wherein the floating gate has dimensions less than 10 nanometers by 10 nanometers by 10 nanometers after oxidation.

95. The method of claim 93, wherein the floating gate has dimensions less than 30

nanometers by 30 nanometers by 30 nanometers after oxidation.

96. The method of claim 93, wherein the floating gate has dimensions less than 10 nanometers by 10 nanometers by 10 nanometers after the floating gate is oxidized to reduce its size, and greater than 10 nanometers by 10 nanometers by 10 nanometers before the floating gate is oxidized to reduce its size.

97. The method of claim 87, wherein the width of the channel region is less than 70 nanometers.

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98. The method of claim 87, wherein the first gate dielectric layer has a thickness of about 1 nanometer.
99. The method of claim 87, wherein the floating gate is formed using electron beam lithography.

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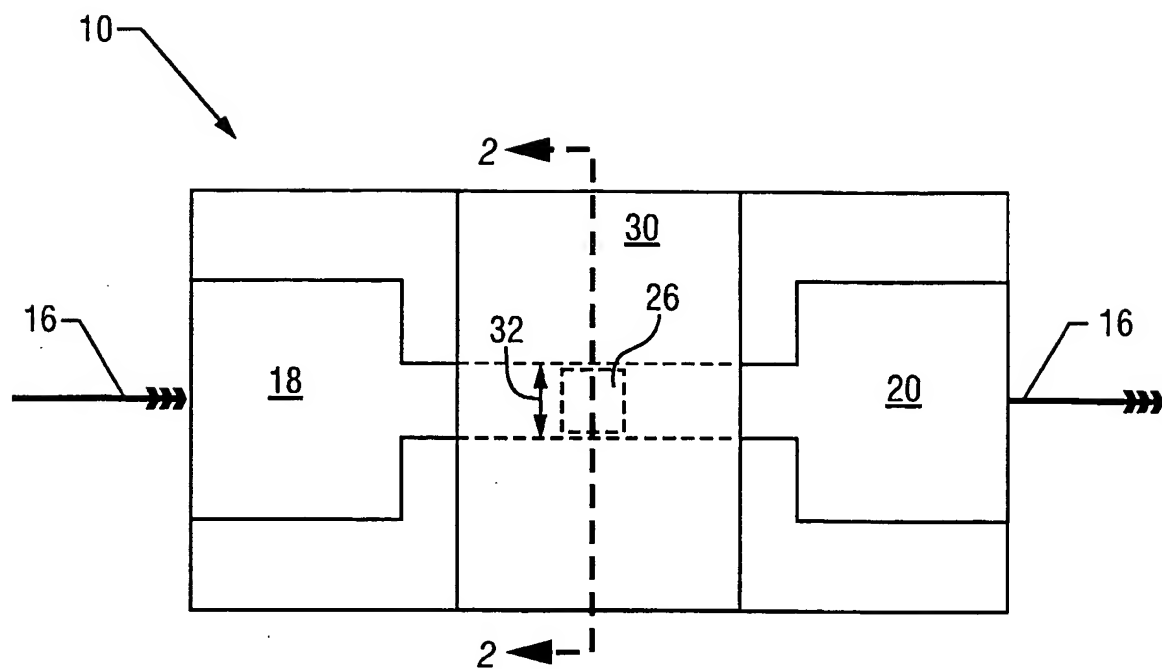


FIG. 1

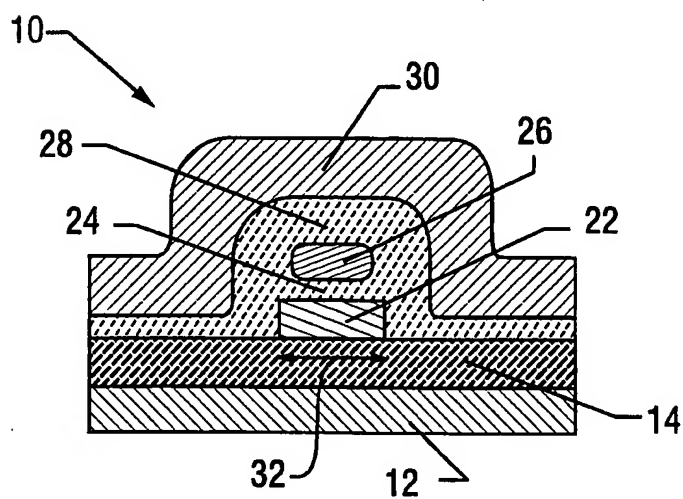


FIG. 2

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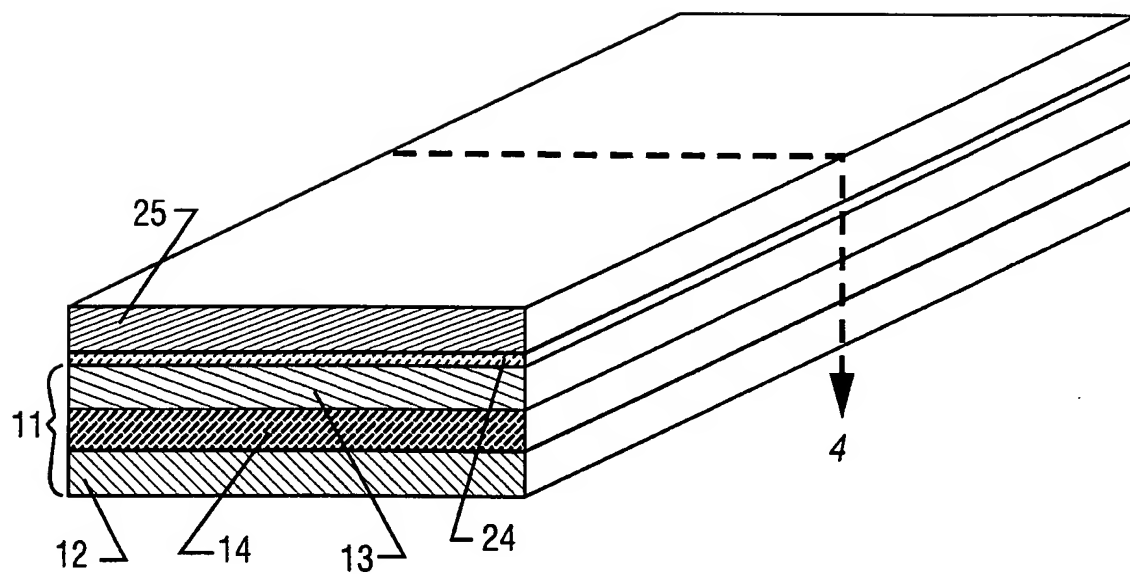


FIG. 3

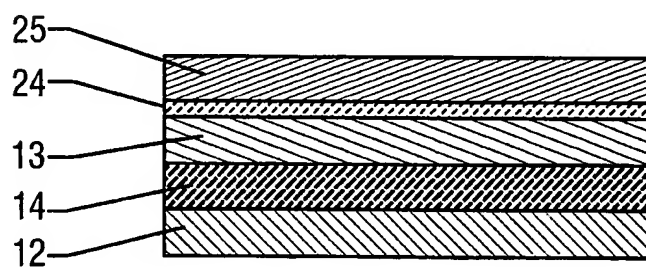


FIG. 4

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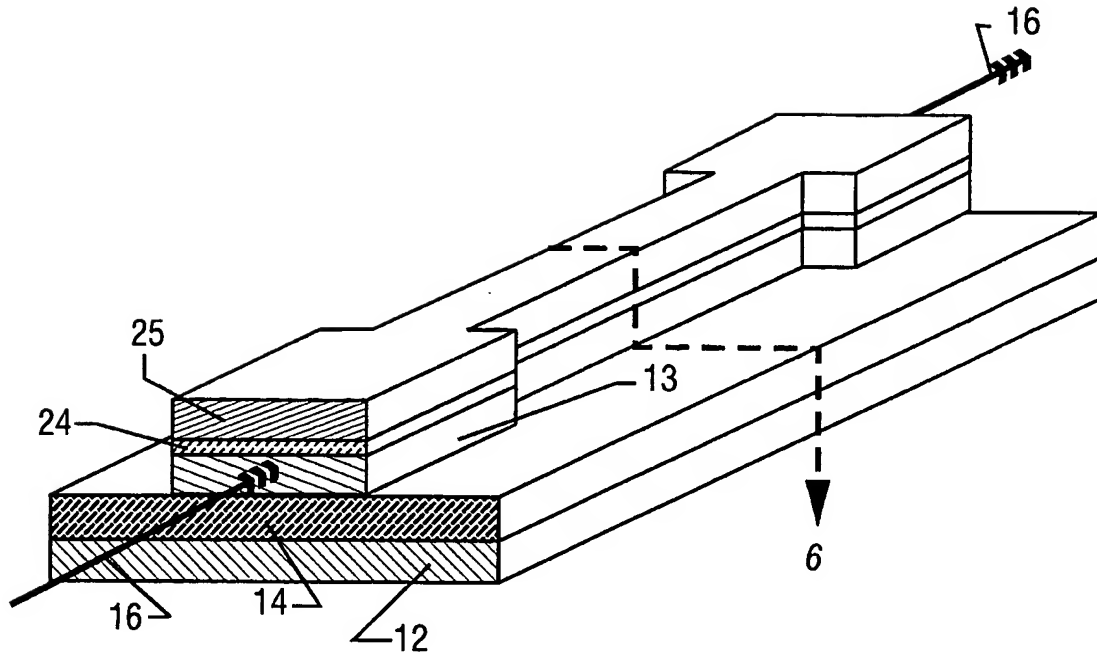


FIG. 5

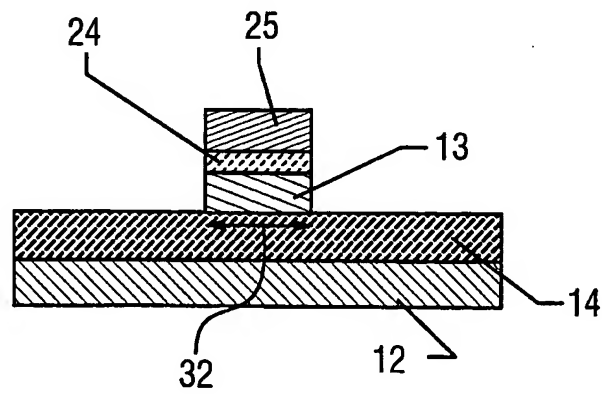


FIG. 6

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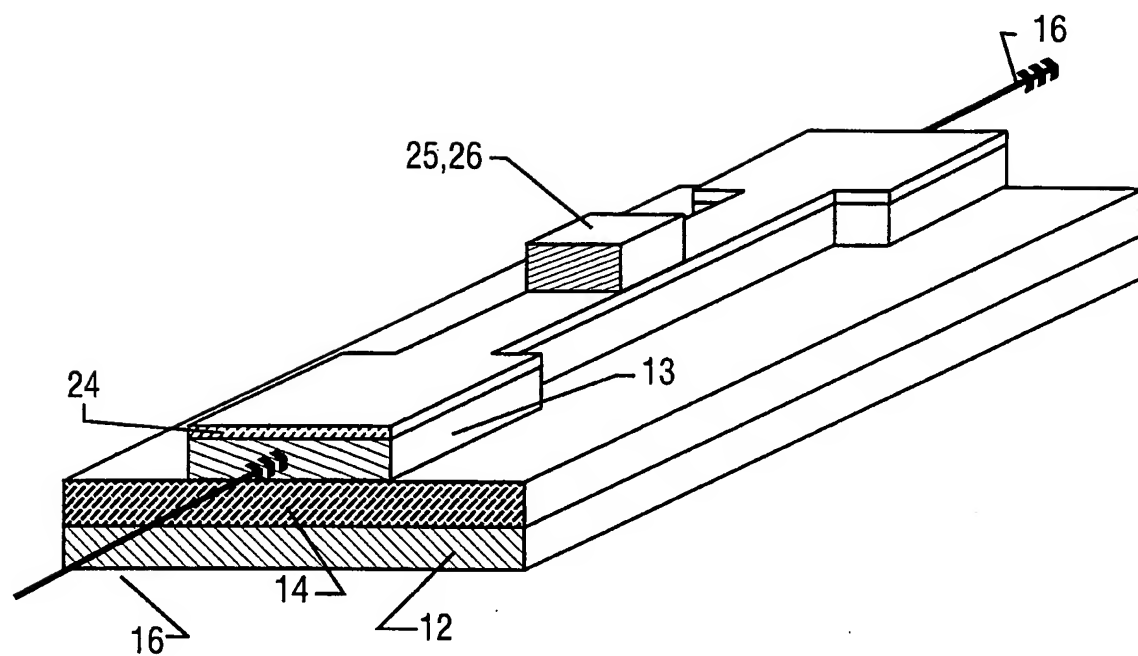


FIG. 7

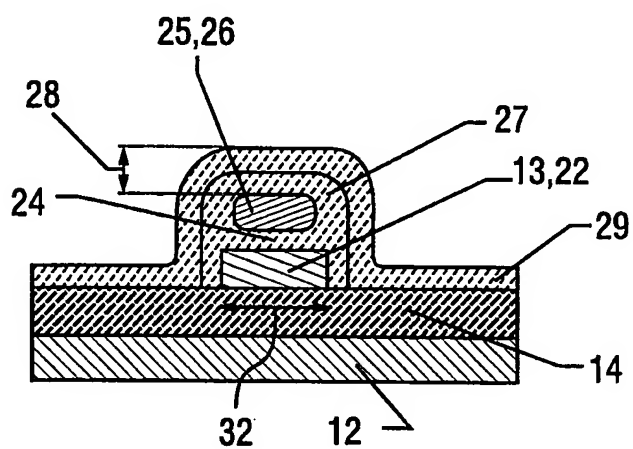


FIG. 8

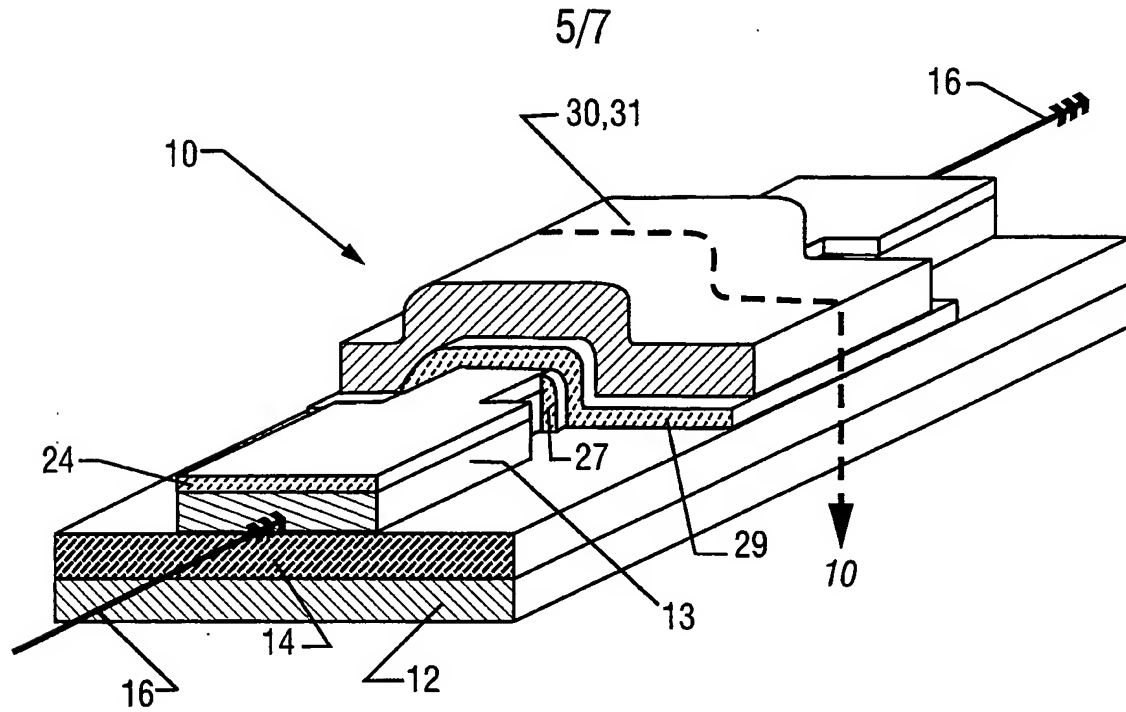


FIG. 9

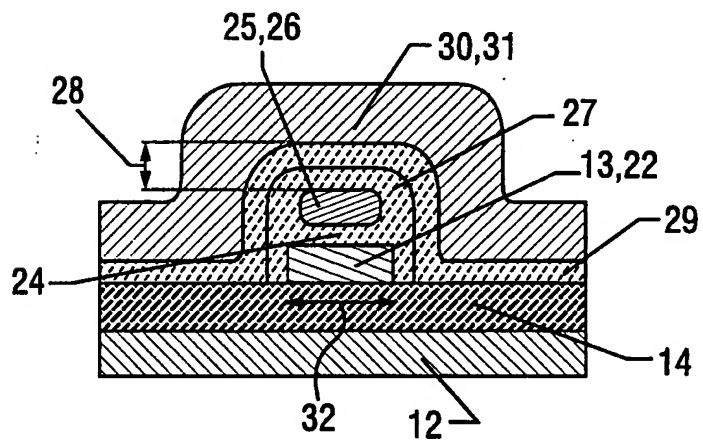


FIG. 10

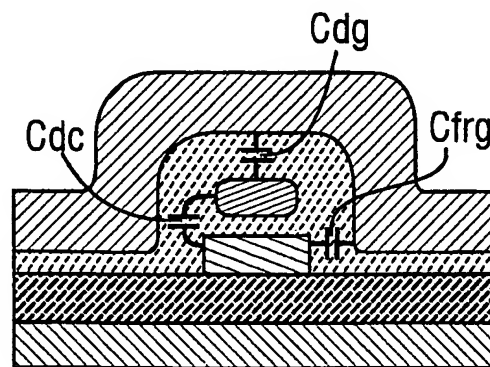


FIG. 16

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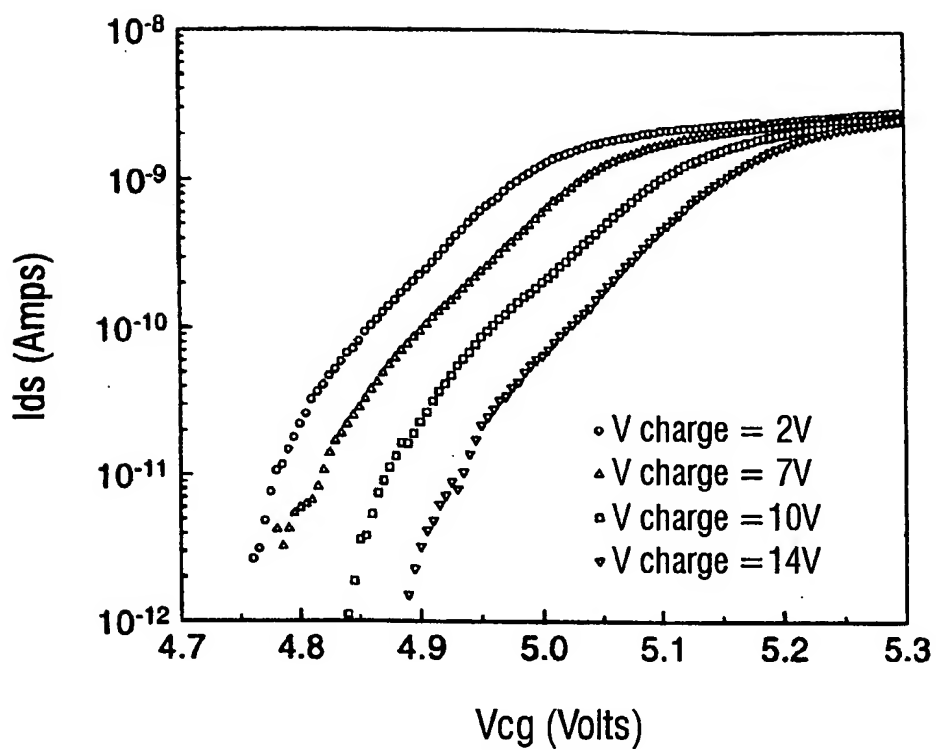


FIG. 11

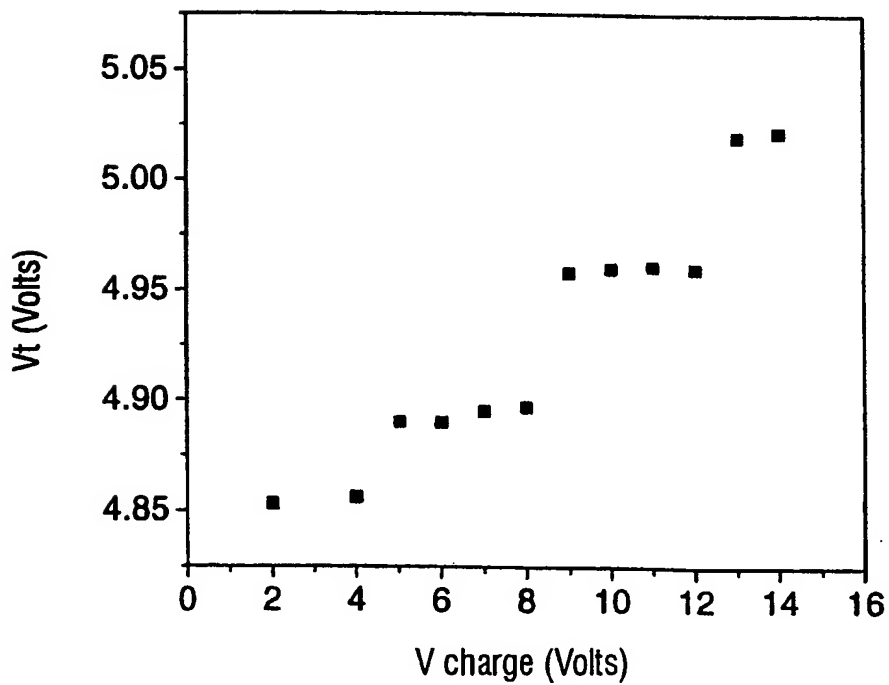


FIG. 12

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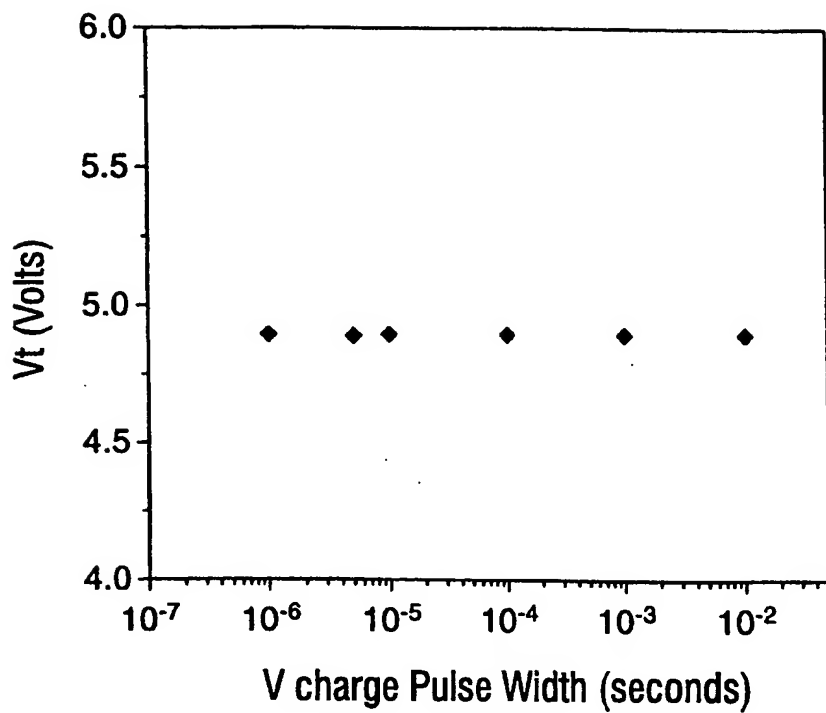


FIG. 13

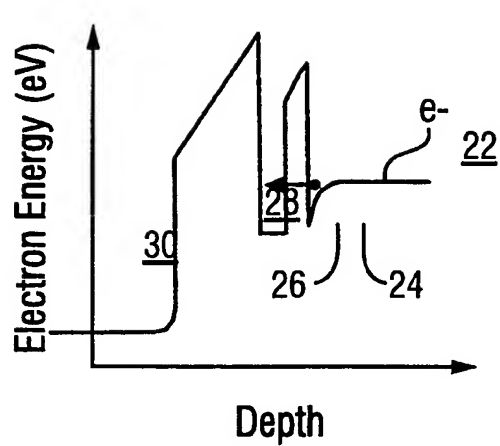


FIG. 14

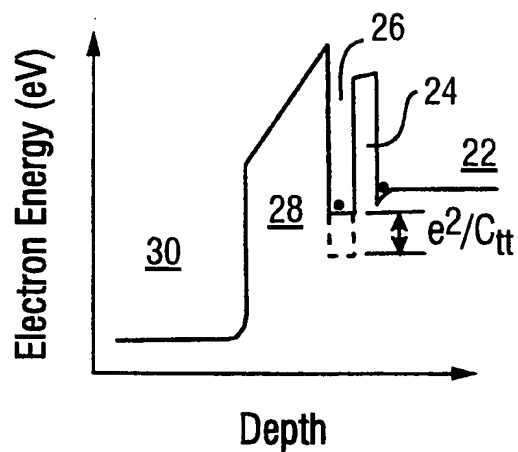


FIG. 15